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That Provides The Gearbox Capability To Decouple The Memory Clock Rate From The Logic-fabric-based Controller Clock Rate At An Appropriate Ratio. This 4th, 2024
Keystone II Architecture DDR3 Memory Controller (Rev. C) Keystone II Architecture DDR3 Memory Controller User's Guide Literature Number: SPRUHN7C October 2013–Revised March 2015. ...
4.41 PHY Timing Register 0 (PTR0)..... 2th, 2024
Xilinx WP383 Achieving High Performance DDR3 Data Rates In ... Figure 5: PHY Architecture And Data Transfer To The Logic-Fabric-Based Memory Controller Logic Fabric Memory Controller PLL PHY_CONTROL PHASER_IN Generates Capture Clock Using DQS. PHASER_OUT Generates Outgoing DQS. PHASER_IN
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