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Sin Encoder - Mixed-signal And Digital Signal Processing ICs

Digital I/O Unit Encoder Interface Event Capture Unit Watchdog Timer

PM ROM 2k X 24 DM RAM 1k X 16 PM RAM 2k X 24

MEMORY SERIAL PORTS SPORT0 SPORT1 Precision Voltage Reference Power On Reset

EXTERNAL ADDRESS BUS EXTERNAL DATA BUS

Figure 4: Block Diagram For The A

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Cable Network Element B Tx OUT X-IN Rx IN Out MON
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Cables And Cross-connect Jumpers Is Addressed At The
DSX Bay Framework, Ensuring An Organized And E Jun
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