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Detailed Simulation Results

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In This Section We Describe The Design Of The first Pro-otype Of Our Simulator. It Consists Of A Very Simple Network Simulator And A Wrapper Library For The MPI Calls. We Will Describe The Simulator And The Wrapper Library In The Next Two Sub-sections, And F 3th, 2024

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4 Fault Simulation Scenario Circuit Model: Mixed-level Mostly Logic With Some Switch-level For High- Impedance (Z) And Bidirectional Signals High-level Models (memory, Etc.) With Pin Faults Signal States: Logic Two (0, 1) Or Three (0, 1, X) States For Purely Boolean Logic Circuits Four States (0, 1, X 3th, 2024

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