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Mum Speedup Can Occur At 1 Big Core, N Base Cores, Or With An Intermediate Number Of Middle-sized Cores. Consider,  $N=16$ . With  $F=0.5$ , One Core (of Cost 16 BCEs) Gives The Best Speedup Of 4. With  $F=0.975$ , 16 Single-BCE Cores Provide A Speedup Of 11.6. With  $N=64$ ,  $F=0.9$ , 9 Cores Of 7.1 BCEs Each Provides An Overall Speedup Of 13.3. Imp Jan 6th, 2024

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Continental, DaimlerChrysler, Ford, Toyota and Volkswagen[2]. Today, 9 Core Partners, 50 Premium Members, 78 Associate Members And 21 ... (SWC) That Each Of Which Contain One Or More Runnable. Each SWC Is An Ap- ... The Sender/receiver

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- IPC – Inter-processor Communication
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The AM57x Family Of System-on-chip (SoC) Jun 13th, 2024

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Few-mode Multicore fibers For Long-haul Transmission Line Yusuke Sasaki A, ↑ , Katsuhiro Takenaga A , Shoichiro Matsuo A , Kazuhiko Aikawa A Mar 8th, 2024

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The Application Flow That Is Not Parallelizable. This Can, For Example, Be A Set Of TCL Scripts That Are Used For Specific Specialized Reporting Purposes. Since The Execution Of These Scripts Is Often Not Parallelized, They Impact The Gains Achievable From Multicore Computing. The Application May 3th, 2024

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