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Condition Mainly Used With Binary Logic Elements Where The Logic State 1 (TRUE) Is Converted To A Logic State 0 (FALSE) Or Vice Versa [IEC 60617-12, IEC 61082-2] 3.20 Logic Inversion Condition Mainly Used With Binary Logic Elements Where A Higher Physical Level Is Converted To A Lower Physical Level Or Vice Versa [Mar 27th, 2024

Two Classes Signals Deterministic Signals & Random Signals

˜˜Note˜˜ Keep In Mind That Rand Gives Numbers In (0,1), That Is, 0 < Rand