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Series Size Code In Inch (in Mm) Structure Min. Max. Min. Inductance Range Rated Current Max.

DFE18SAN_E0 DFE18SAN_G0 DFE18SBN_E0 DFE201208S DFE201210S DFE201210U DFE201610C DFE201610E DFE201610P DFE201610R DFE201612C DFE201612E DFE201612P DFE201612R DFE252007F DFE252008C 5th, 2024

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9 Chip Bonding At The First Level - The Chip Collection

Of Failure For An IC. 26% Of All IC Failures Are Related To The Wirebond. Figure 9-3 Shows The Fail-ure Mechanism Breakdown For Packaged Die. Chip Bonding At The First Level INTEGRATED CIRCUITENGINEERING CORPORATION 9-3 Source: ICE, "Roadmaps Of Packaging Technology" 22510 Wirebond TAB Flip 6th, 2024

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V.2.-.1 Chip Mainboards: Nec/Renesas: 1 Chip ASRock: X58 Chipset: P55 Chipset: X58 Extreme3 P55 Deluxe3 ... AM3+ Chipset: AM3 Chipset: 890GX Extreme3 870 Extreme3 880G Extreme3 M3A790GXH/USB3 . Mainboard Chip ... 7th, 2024

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